ABSTRACT

An analog input signal A1 is held by a sample-hold-amplifier (SHA) 12 to be outputted as a voltage V12. The V12 is converted into a digital signal of 1,5 bits by sub-A / D converters (SADC: comparators 13, 14, and an encoder 15), and the digital signal is further converted into an analog signal by sub-D / A converters (SDAC: switches 16a, 16b, 16c) to be delivered to an SHA 18. The SHA 18 amplifies a difference in voltage between the voltage V12 and the SDAC by a factor of two to thereby output a voltage VA, which is delivered to an analog-to-digital conversion stage 20. By so doing, the range of an input voltage of the respective SHAs is suppressed to 1 / 2 of that for the conventional case, thereby enabling high-speed operation to be executed without impairing linearity.